Claim 11 has been objected to due to a noted informality. However, Applicant has already amended claim 11 to correct the informality in the Amendment submitted on May 30, 2002. Acknowledgement of this correction is respectively requested.

Claims 1, 2, 7 and 40-42, 46 and 48-51 have been rejected under 35 U.S.C. §102(b) in view of Kinzer (U.S. 5,644,148). For reasons that will now be discussed, these claims are allowable over Kinzer.

In general, there is a need to increase the capacity of electric current in integrated IGBT or DMOS chips. This can be done by increasing the chip area. However, increasing the chip area increases waste and reduces yield when a defect occurs. The claimed invention provides a way of salvaging chips that include defects.

Independent claim 1 recites that the gate electrodes of one cell block are electrically independent of the gate electrodes of the other cell blocks. Therefore, it can be determined whether each of the cell blocks is defective or not by, for example, measuring a withstand voltage between each gate electrode and emitter electrode. That is, the withstand voltage of each of the cell blocks is measured by applying voltage through each of the gate electrodes. The cell block is non-defective when the withstand voltage is a predetermined voltage or more, and is defective when the withstand voltage is lower than the predetermined voltage (page 11, lines 1-15).

Based on the determination of defective ones of the cell blocks, only gate pads of non-defective cell blocks are connected with a gate terminal provided outside of the semiconductor substrate. The gate pads of defective cell blocks are not connect with the gate terminal. In this way, semiconductor chips including defects can be salvaged.

Kinzer discloses in FIG. 19 a semiconductor substrate (50), a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes (G) respectively provided

in the plurality of cell blocks, and a gate pad are provided on the semiconductor substrate and connected with the plurality of gate electrodes. Further, Kinzer discloses plural gates (polysilicon segments 113-115). However, even though not well shown in FIG. 19, the plural gates are connected with each other because the plural gates are patterned in a hexagonally shape grid on P^- and N^+ layers. That is, in column 11, lines 45-51 of Kinzer, which explains manufacturing processes of a semiconductor device illustrated in FIG. 19, states as follows:

> As shown in FIG. 15, this exposes the remaining polysilicon web and the surface of the silicon substrate 52 inside the windows 98, 99 and 100. Note that this photolithograph-etch step leaves in place oxide islands 83, 84 and 85, as well as the hexagonally shaped grid represented by gate oxide and polysilicon segments respectively 110, 111, 112 and 113, 114, 115.

Further, Kinzer discloses a polysilicon gate segments overlying gate oxide web that extend over at least P- channel regions (column 6, lines 29-38). Although Kinzer discloses a semiconductor device having a common gate electrode connected to all gates (FIG. 2, column 6, lines 45-47) that is basically the same configuration as in FIG. 19, Kinzer fails to disclose cell blocks that each have a gate pad, as recited in all independent claims of the present invention. Referring specifically to the language of claim 1, Kinzer fails to show gate electrodes of one cell block that are electrically independent of those of other cell blocks. Therefore, as Kinzer does not anticipate claims 1 and 40, and claims 3, 7 and 41, 42, 46, and 48-51 that depend therefrom, Applicant respectfully requests that the Examiner's §102(b) rejection based on Kinzer be withdrawn.

Claims 3 and 16-19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Smith (U.S. 6,329,692) and Kohno (U.S. 6,180,966). This rejection is respectfully traversed.

Claims 3 and 16-19 recite that the non-defective first cell block is connected with a gate terminal and a defective second cell block is connected with a ground terminal. Therefore, a gate controlling signal is not fed to the gate electrode of the defective cell block so that elements in the defective cell block are not operated.

Smith discloses in FIG. 4 that a gate of the transistor 42 connects with a ground terminal Vss via resistor 44, and a gate of the transistor 36 connects with a gate terminal V_{DD}. However, the transistor 36 must be formed by a non- defective cell and should be appropriately operated as part of an electric circuit shown in FIG. 4.

Kohno discloses in FIG. 2 a plurality of cell blocks in which the overcurrent can damage the cells. However, the defective portion existing where a cell is formed is basically formed during the substrate formation process, and therefore damage caused by overcurrent flowing in the cells thus represents a different type of damage as opposed to the damage that would result in the plurality of cell blocks in the present invention if gates of defective cell blocks were connected with gates of non-defective cell blocks.

Accordingly, neither Kinzer, Smith nor Kohno discloses a plurality of cell blocks where gate electrodes of one cell block are independent from those of other cell blocks. This feature is important for disabling defective cell blocks without having to discard the entire chip when a defect is present. Thus, even if Smith or Kohno was combined with Kinzer, the present invention as recited in the claims would still not be taught or suggested by the prior art combination.

Claim 5 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Sanchez (U.S. 6,160,305). This rejection is respectfully traversed.

Sanchez discloses in FIG. 1 that a gate of a transistor 20 connects with an output terminal, and a gate of the transistor 16 connects with an emitter terminal of the transistor 12, to create an emitter potential. However, the transistor 16 must be formed by a non- defective cell and should be appropriately operated as part of an electric circuit shown in FIG. 5. Thus, even if Sanchez was combined with Kinzer, the present invention as recited the claims is not taught or suggested by the prior art combination as the same reason as discussed in connection with claims 3 and 16-19.

Claims 8-15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Calhoun (U.S. 4,631,569). This rejection is respectfully traversed.

Claim 8 recites that a plurality of marks is respectively provided on the cell blocks to distinguish whether each of the cell blocks is defective. Therefore, it can be easily determined via the marks whether the gate pads are connected with the non-defective cell block or the defective cell block. Accordingly, the gate pads connected with the non-defective and defective cell blocks can be respectively connected with different terminals.

Calhoun discloses a plurality of circuit cells in which the defective cells are marked to be distinguished from the working cells. However, again, Calhoun fails to disclose a plurality of cell blocks where gate electrodes of one cell block are independent from those of other cell blocks. Thus, even if Calhoun was combined with Kinzer, the present invention as recited in the claims would not be taught or suggested by the combination.

Claim 20 has been rejected §103(a) as being unpatentable over Kinzer in view of Smith, Kohno and Shinohe (U.S. 5,793,065). This rejection is respectfully traversed.

Claim 20 recites that the plurality of cell blocks includes a first group of cell blocks, which have an equal threshold voltage and are connected with the gate terminal, and a second group of cell blocks, which have different threshold voltages from one another and are connected with one of the plurality of pads. That is, the first group of non-defective cell blocks is connected with the gate terminal, while the second group of defective cell blocks is connected with the pads with an emitter potential. Therefore, elements in the non-defective cell block are operated and elements in the defective cell block are not operated.

Shinohe discloses that the use of adjacent elements having different threshold voltages reduces the adverse influence of threshold voltage differences among the elements. However, in such a configuration, the different threshold voltages are intentionally formed to reduce the adverse influence. This feature is different from that recited in claim 20. Further, Shinohe fails to disclose a plurality of cell blocks where gate electrodes of one cell block are independent from those of other cell blocks. Therefore, Shinohe fails to cure the shortcomings of Kinzer, Smith, and Kohno. Thus, even if these references were combined, the terms of the claims would not be satisfied by the resulting configuration.

Claims 38 and 39 have been rejected §103(a) as being unpatentable over Kinzer in view of Smith and Crane (U.S. 6,339,191). This rejection is respectfully traversed.

Regarding claims 38 and 39, these claims are different from Kinzer as mentioned above. Crane discloses trays for carrying dies. However, Crane fails to disclose a plurality of cell blocks where gate electrodes of one cell block are independent from those of other cell blocks. Therefore, even if Smith and Crane were combined with Kinzer, the terms of the claims would not be satisfied by the prior art combination.

Claims 43-45 and 47 have been rejected §103(a) as being unpatentable over Kinzer. This rejection is respectfully traversed.

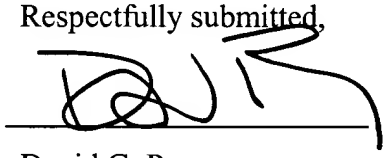
Claims 43-45 and 47 depend from independent claim 40; therefore, these claims are different from Kinzer as mentioned above. That is, independent claim 40 recites a plurality of transistor cells that are divided into groups. The cell groups of claim 40 are the same as the cell blocks of claim 1. Claim 40 also recites a plurality of common gate electrodes for the groups, respectively. The word "respectively" indicates that each group has a separate common gate electrode. This feature is not taught or suggested by Kinzer.

Accordingly, Applicant respectfully requests the Examiner's §103 rejection of claims 43-45 and 47 be withdrawn.

In view of the above amendments and remarks, the present application is now believed to be in condition for allowance. A prompt notice to that effect is respectfully requested.

A petition for 1-month extension of time is enclosed. Please change any additional unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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